REMARKS

By this amendment, Applicants have amended the claims to more clearly define their invention. In particular, claims 1 and 2 have been amended to clarify that the protrusion is a loop-shaped protrusion disposed in a loop surrounding an area overlapping the bonding opening to be sealed and has generally flat plate-shaped surfaces in areas within and outside the loop-shaped protrusion recessed from the loop-shaped protrusion. Applicants have also added claims 5-12 to define further aspects of the present invention. The amendments to claims 1 and 2 and new claims 5, 7, 9 and 11 are supported by, e.g., Figures 3, 4, 5 and 8 and the description at page 8, line 28, to page 9, line 2 and page 11, lines 8-10 of Applicants' substitute specification. New claims 6, 8, 10 and 12 are supported by, e.g., Figure 8 and the description at page 11, line 10 to page 12 of Applicants' substitute specification.

The Examiner's comments in numbered section 2 of the Office Action with respect to the Information Disclosure Statement filed November 7, 2006 are noted. The documents submitted with the Information Disclosure Statement are the same documents used by the Examiner in rejecting the claims in the outstanding Office Action, i.e., JP 2002-363361 to Kawanobe et al. and JP 200-329811 to Inoue et al. Since these references have been applied by the Examiner, it is requested that the Examiner list these references on a Notice of References Cited (PTO-892). Should the Examiner prefer Applicant's to provide a form PTO/SB/08A, the Examiner is requested to so advise the undersigned and a completed form will be provided.

Claims 1-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kawanobe et al. in view of Inoue et al. Applicants traverse this rejection and request reconsideration thereof.

The present invention relates to a mold die and to a method for manufacturing a semiconductor device by sealing, by transform mold processing using a die. The present invention can be used for sealing a semiconductor chip mounting on the surface of a wiring board via an elastic material. As shown, e.g., in Figure 2, such a wiring board has a plurality of openings including a bonding opening 4. The semiconductor chip 3 can be mounted on the surface of the wiring board via an elastic material 2. Applicants have found that bending or distortion can be generated around the bonding the opening 4 and that any such bending or distortion may allow insulating resin which flows into the bonding opening 4 to leak into the space formed between the bottom die and the insulating substrate, as shown in Figure 11. The thin insulating substrate (101) can not bear the injection pressure from the flow of the insulating resin and may float. As a result, the insulating resin 5 may be spread over the surface of the insulating substrate 101, as shown in Figure 12, and may spread over the area of the external terminal openings 101A and flow therein causing poor electrical conduction between the external connecting terminals and the conductive pattern.

The present invention solves the problems Applicants have found with the prior art by using a die which includes a loop-shaped protrusion disposed in a loop surrounding an area overlapping the bonding opening to be sealed with the insulating resin and has generally flat plate shape surfaces in areas within and outside the loop-shaped protrusion. See, e.g., Figures 3, 4, 5 and 8. The loop-shaped protrusion presses the wiring board toward the semiconductor chip around the area overlapping the bonding opening.

For the reasons set forth from page 9, line 16 to page 11, line 5 of the substitute specification, the use of the loop-shaped protrusion disposed around an area overlapping the bonding opening, especially in combination with mounting the

semiconductor chip on the surface of the wiring board via an elastic material, can greatly improve yield in manufacturing the semiconductor device.

The published Japanese patent application to Kawanobe et al. discloses a semiconductor device and manufacturing method in which, to prevent degradation of reliability in a semiconductor device, a semiconductor chip is mounted by interposing an elastic material on a wiring board and the circumference of a semiconductor chip is sealed with an insulating material. As recognized by the Examiner at page 4, lines 2-4 of the Office Action, "Kawanobe fails to disclose a second die comprising a protrusion disposed around an area overlapping the bonding opening to be a sealed with the insulating resin."

The Examiner cites Inoue et al. as alleging disclosing "a second die 10B comprising a protrusion (i.e. the portion attached directly to the substrate 3) disposed around an area overlapping the bonding opening to be sealed with an insulating resin." However, rather than showing the presently claimed protrusion, it appears the member 10B in Inoue et al. (see Figure 3) does not have the presently claimed loop-shaped protrusion but only a recess under Au wires 6 or 26. According to the present invention, the second die has a loop-shaped protrusion disposed in a loop surrounding an area overlapping the bonding opening and has generally flat plate-shaped surfaces in areas within an outside of the loop-shaped protrusion recessed from the loop-shaped protrusion. Even if the Examiner is interpreting the raised area the recess in number 10B of Inoue to be a protrusion, it is submitted the member 10B does not correspond to the second die of the present invention since it does not have a loop-shaped protrusion disposed in a loop surrounding an area overlapping a bonding opening and the generally flat plate-shaped surfaces in areas within and outside the loop-shaped protrusion recessed from the loop-shaped protrusion.

Accordingly, even assuming, arguendo, one of ordinary skill in the art would have reason to combine the teachings of Kawanobe et al. and Inoue, it is submitted even the combined teachings would not have rendered obvious all of the features of the present invention presently claimed.

Accordingly, the presently claimed invention is patentable over the proposed combination and Kawanobe et al. and Inoue et al.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.43552X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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